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Physical planning of on-chip interconnect architectures

Hongyu Chen   Bo Yao   Feng Zhou   Chung-Kuan Cheng
Dept. of Comput. Sci. & Eng., Univ. of California, La Jolla, CA, USA

Abstract
Interconnect architecture plays an important role in determining the throughput of meshe
structures. We assume a mesh structure with uniform communication demand for commu
commodity flow (MCF) model is proposed to find the throughput for several different routii
experimental results reveal several trends: 1. The throughput is limited by the capacity of
column in the mesh, simply enlarging the congested channel cannot produce better throt
shape provides around 30% throughput improvement over a square chip of equal area. 2
allows 17% throughput improvement over 90-degree mesh and a 90-degree and 45-degri
provides 30% throughput improvement. 3. To achieve maximum throughput on a mixed M
diagonal **interconnect** architecture, the best ratio of the capacity for diagonal routing layε
for Manhattan routing layers is 5.6. 4. Incorporating a simplified via model, interleaving diε
and Manhattan routing layer is the best way to organize the wiring directions on different I

Index Terms
Inspec

    Controlled Indexing
    circuit layout CAD   system-on-chip

    Non-controlled Indexing
    congested channel   diagonal **interconnect** architecture   flexible chip shape   mε
    meshed communication structures   mixed Manhattan **interconnect** architecture
    commodity flow model   on-chip **interconnect** architectures   physical planning   i
    via model
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